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The Intel Lithography Roadmap

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Peter J. Silverman, Technology and Manufacturing Group, Intel Corporation

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ABSTRACT

Lithography is the primary enabling technology for semiconductor manufacturing. Having led the industry transition to Deep Ultra-Violet (DUV) lithography, Intel is currently leading the transition to 193nm, 157nm, and Extreme Ultra-Violet (EUV) lithography. Lithography technologies, such as 193nm, 157nm, and EUV lithography, which have benefited from Intel investment, have gained industry acceptance, while competing technologies, such as xray lithography, are no longer being pursued.

The Intel Lithography Roadmap is the Intel plan for the next several generations of lithography technology. In this paper, we discuss this roadmap and review the strategic and tactical forces that have produced the current version of this roadmap. The status of future lithography technologies is also reviewed, with an emphasis on 193nm, 157nm, and EUV lithography. Finally, the key question of affordability is addressed.

INTRODUCTION

Lithography is the single most important driver of Moore's law. By providing the capability to continuously reduce the size of features patterned on semiconductor wafers, each new generation of lithography equipment has enabled faster microprocessors and smaller, less costly integrated circuits. Without the continuous improvements in lithography process and equipment technology that have occurred over the past 30 years, personal computers, cell phones, and the Internet would not be available today.

Due to the importance of lithography, Intel devotes large amounts of time and money to developing a strategic and tactical roadmap for the future direction of Intel lithography technology. Because the semiconductor industry has aligned with the Intel Lithography Roadmap, Intel's decisions have a strong influence on the investment decisions made by the suppliers who provide lithography equipment to the semiconductor industry. For example, Intel leadership was the catalyst for industry

investment in 157nm lithography. Similarly, Intel has been the force behind the semiconductor industry acceptance of EUV lithography as the successor to traditional optical lithography. The strong influence of the Intel Lithography Roadmap makes it worthwhile to review both the roadmap and the forces that have created it.

The Intel Lithography Roadmap is driven by technical forces such as lithographic resolution and process control; tactical forces such as the development schedule for new lithography equipment; and commercial forces such as the affordability of lithography equipment. A review of these forces explains how the current Intel Lithography Roadmap has been developed. Intel has made the decision to invest in certain lithography technologies, such as 193nm, 157nm, and EUV lithography and not to invest in other technologies, such as xray lithography and electron projection lithography. A review of the status and timing of future lithography technologies provides insight into the decisions Intel has made in the past and will make in the future.

It is well known that the cost of lithography equipment has increased at a nearly exponential rate over the past 30 years. The \$100,000 contact printers of the early 1970s have given way to the over \$12M 193nm step-and-scan exposure tools of the first decade of the 21st century. How will the semiconductor industry be able to afford such costly equipment? Will the investment in future lithography technologies be wasted because of other limitations on transistor size reduction (transistor scaling)? Intel has a high degree of confidence in the ability of the industry to continue transistor scaling for many years into the future. Furthermore, Intel has a well-developed strategy to manage lithography affordability. This strategy will enable continued transistor scaling.

This paper reviews the strategic decisions and thinking that have resulted in today's Intel Lithography Roadmap. The status of advanced technologies such as 193nm, 157nm, and EUV lithography are reviewed in order to provide the background for Intel's roadmap decisions. Information is presented to support the continuing need

for advanced lithography technologies to enable transistor scaling. Finally, the affordability of future lithography technologies is addressed.

INTEL LITHOGRAPHY ROADMAP

The Intel Lithography Roadmap is the plan for the lithography technology that will be used to pattern the smallest features on each new generation of integrated circuits. Contemporary semiconductor devices have ~25 patterned layers. The smallest features are on the four to six “critical” layers, which define the size of the transistors. The remaining layers are used to interconnect the transistors to form an integrated circuit. Interconnect layers have larger feature sizes. As discussed in the section on affordability, the interconnect layers are normally patterned by “reusing” lithography equipment from earlier process generations.

Intel always uses the most advanced lithography technology that is ready for manufacturing to pattern critical layers. As shown in Figure 1, Intel is using DUV (248nm) lithography for the critical layers of the 130nm generation. The Intel plan is to transition to 193nm lithography for the 90nm generation; 157nm will be used on the critical layers of the 65nm generation if 157nm lithography is ready on time, and 157nm lithography will be used on the critical layers of the 45nm generation if EUV is not ready on time.

The dates shown in Figure 1 are for the start of high-volume manufacturing. However, lithography tools for process development are required at least two years sooner. Furthermore, equipment suppliers require approximately five years to design and build each new generation of lithography equipment. Therefore, the ten-year look-ahead provided by the roadmap is needed to

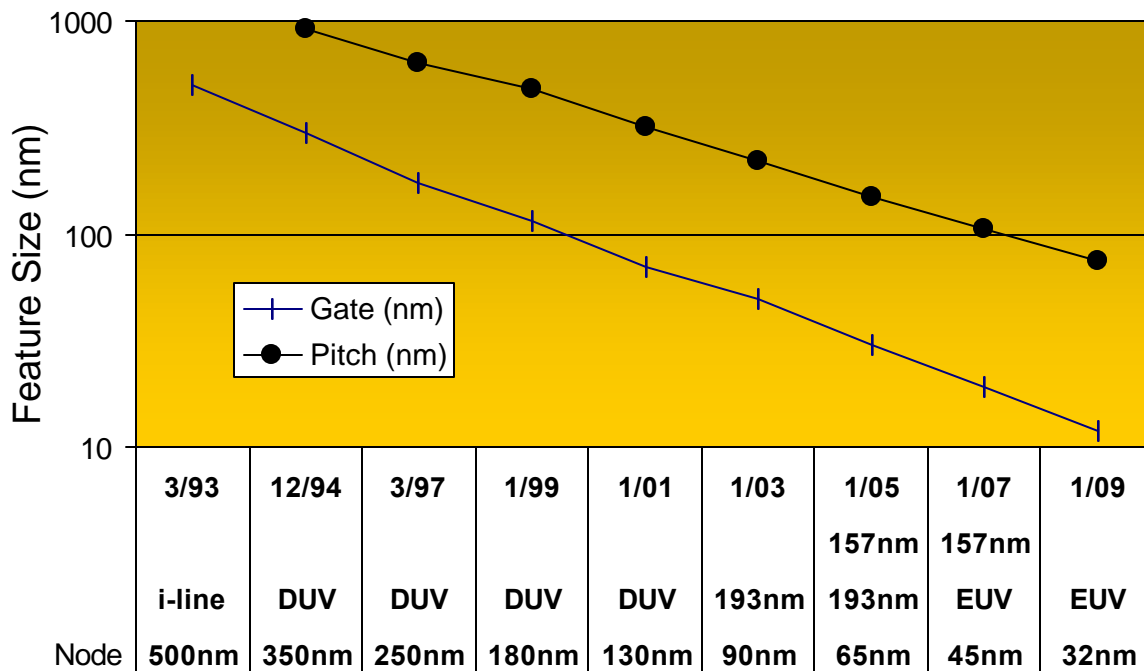


Figure 1: Intel Lithography Roadmap

The Intel Lithography Roadmap shows a continuous progression to shorter lithography wavelengths (smaller). Starting with i-line (365nm) lithography, the roadmap progresses to DUV (248nm), 193nm, 157nm and EUV (13nm) lithography. The drive to shorter wavelengths is because optical resolution is directly proportional to wavelength. Using a shorter wavelength enables manufacturing integrated circuits with smaller transistors.

allow both Intel and the equipment suppliers to plan for the future.

Strategic and Technical Drivers

For nearly 30 years the growth of the semiconductor industry has been tied to Moore’s Law; the essence of which is the ability to give customers faster, more complex products by manufacturing faster, more complex

integrated circuits, at a constant or decreasing price. The Intel Lithography Roadmap is driven by a commitment to maintain the industry momentum provided by Moore’s Law.

In lithographic terms, Moore’s Law translates into three technical requirements:

1. *Reduce pitch by 30% every two years.* A 30% reduction in pitch produces a 50% reduction in chip area. This allows more complex products to be produced without an increase in chip size.
2. *Reduce gate width by >30% every two years.* Since transistor speed is inversely proportional to gate width, smaller gates mean faster chips.
3. *Maintain a constant cost for lithography.* Since lithography is the largest single component of chip fabrication cost, lithography costs must stay constant to allow chip costs to stay constant.

Figure 1 shows the 30%/generation pitch and gate size reduction, which Intel has maintained on a two-year cycle for the past ten years.

Intel’s roadmap strategy is designed to ensure that these requirements are met for each new generation of Intel technology. Therefore, lithography decisions are based on staying on the two-year cycle of Moore’s Law and on meeting device density and speed requirements with affordable lithography technology.

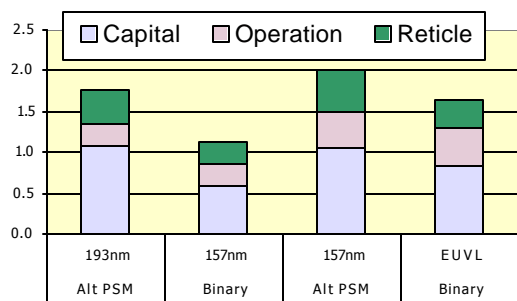


Figure 2: Binary vs. PSM cost/layer

Intel Roadmap Strategy

Semiconductor manufacturers follow two different roadmap strategies. Some companies work very hard to extend their existing, in-use lithography technology for as many generations as possible. Other companies transition as rapidly as possible to each new generation of lithography technology. Intel follows both strategies simultaneously. For the critical, transistor device layers, the Intel strategy is to transition as rapidly as possible to each new generation of lithography technology. For the

less critical, interconnect layers, the Intel strategy is to reuse existing lithography equipment.

Intel transitions rapidly to new lithography technologies because we have found that this is the lowest total cost approach. Even though new generations of lithography equipment are more costly, the costs are more than offset by the savings in other areas; e.g., mask costs.

Figure 2 compares two potential candidates for the critical layers of the 65nm technology node (157nm with Binary masks and 193nm with Alternating Phase Shift Masks) and two candidates for the 45nm node (EUV Lithography with Binary masks and 157nm with Alternating Phase Shift Masks). In both cases, the next-generation technology has significantly lower cost/layer due to less expensive masks and lower capital costs. (The lower capital costs are due to the higher run rate that is achievable with binary masks.) Therefore, Intel’s plan is to use 157nm lithography on the 65nm node and to use EUV Lithography on the 45nm node. Of course, these plans are dependent on the availability of 157nm and EUV exposure tools in the required time frames.

Lithography Roadmap Acceleration

As shown in Table 1, i-line/g-line lithography was used for six technology generations over a period of fifteen years. DUV lithography will be used for three process generations over a period of six years. The Intel Lithography Roadmap (Figure 1) shows 193nm, 157nm, and EUV all being introduced in the following four years. What has happened to force the roadmap to accelerate so rapidly?

Table 1: Wavelength “Generations”

Year	Node	Lithography
1981	2000nm	i/g-line Steppers
1984	1500nm	i/g-line Steppers
1987	1000nm	i/g-line Steppers
1990	800nm	i/g-line Steppers
1993	500nm	i/g-line Steppers
1995	350nm	i-line → DUV
1997	250nm	DUV
1999	180nm	DUV
2001	130nm	DUV
2003	90nm	193nm
2005	65nm	193nm → 157nm
2007	45nm	157nm → EUV
2009	32nm and below	EUV

Two factors have contributed to the accelerated rate of change in lithography:

1. The transition to sub-wavelength patterning as shown in Figure 3.
2. The finite limit on the Numerical Aperture (NA) of optical systems, which sets a limit on the minimum possible resolution at a particular wavelength, as shown in Figure 4.

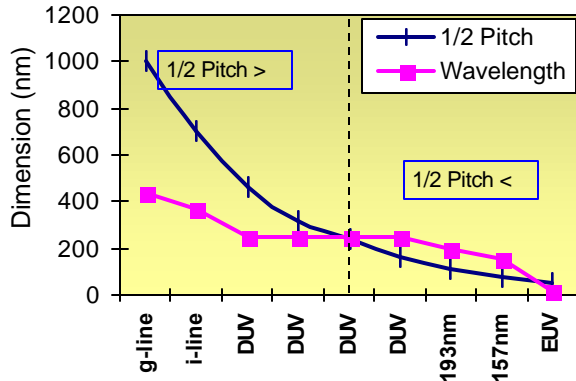


Figure 3: Sub-wavelength lithography

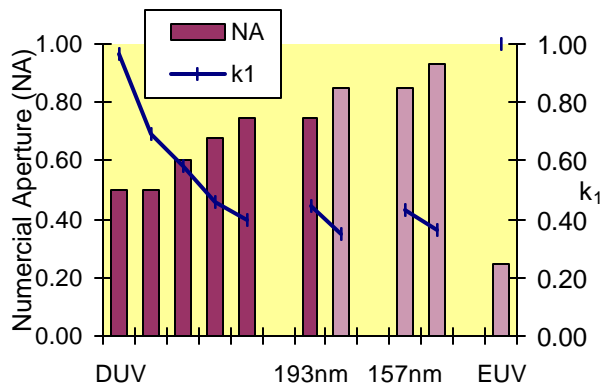


Figure 4: Limits of wavelength extension

Resolution is related to wavelength and NA by the well-known equation:

$$resolution \propto \frac{Wavelength}{Numerical Aperture}$$

The combined impact of these two factors has been to accelerate the rate of introduction of new lithography technologies; i.e., to accelerate the transition to ever smaller wavelengths. The need for smaller wavelengths to maintain Moore's Law is the primary reason that Intel has

invested over \$200M in the development of EUV lithography.

Transistor Scaling

Even if it is possible to use lithography to pattern features smaller than 50nm, there is legitimate concern as to whether other factors will constrain the ability of the semiconductor industry to manufacture 45nm generation and smaller transistors.

Intel has addressed this question by accelerating research on transistor design. The Intel announcement of TeraHertz transistors with gate dimensions below 20nm (Figure 5) clearly demonstrates that transistor physics and material properties will not prevent continuing on the path of Moore's Law. The key issue will be the availability of lithography equipment that can pattern sub-50nm features, in high-volume applications, at affordable costs. This again emphasizes the need to accelerate the lithography roadmap.

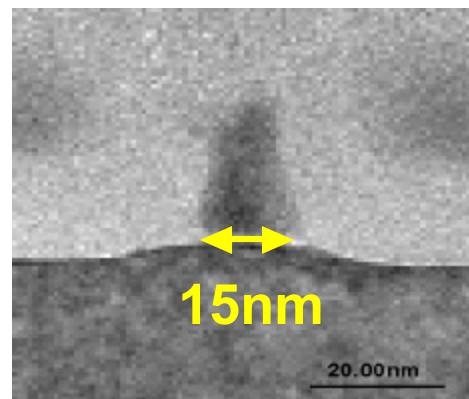


Figure 5: TeraHertz transistor with 15nm gate

TECHNOLOGY DEVELOPMENT STATUS

In the early 1990s, there was significant concern that the industry could not make the transition from i/g-line lithography to 248nm Deep Ultra-Violet (DUV) lithography. There were many challenges to overcome before DUV lithography could be successful in high-volume manufacturing. Exposure tool suppliers had to learn to fabricate precision optics from ultra-pure fused silica. Resist suppliers had to develop and commercialize chemically amplified resists. Mask makers had to learn to use new materials. However, all these challenges were overcome, and DUV (248nm) lithography has been the workhorse technology for semiconductor manufacturing since the 250nm (0.25 micron) generation. DUV exposure tools, which were introduced at 0.50NA, are now in their fourth generation, with fifth-generation, >0.80NA tools due in 2003.

The industry is poised to introduce 193nm lithography into high-volume manufacturing in the second half of 2002. Prototype 193nm exposure tools were delivered in 1996. Early production 193nm tools were delivered in 2001. Both the prototype and early production tools were delivered in small quantities, partly due to the lack of a mature 193nm resist technology. Mature, high-resolution 193nm resists are now available from several suppliers. Lithography equipment suppliers are ready to deliver production quantities of 0.75NA 193nm exposure tools in 2003 to support 90nm integrated circuit manufacturing on 300mm wafers. By early 2003, suppliers will be ready to deliver 0.85NA 193nm exposure tools to support development and early manufacturing of 65nm integrated circuits.

Patterning 65nm generation integrated circuits will require either 157nm lithography or 193nm lithography with Alternating Phase Shift Masks. Both Intel and the lithography equipment suppliers are confident that the cost of 157nm lithography will be less than the cost of 193nm lithography with Alternating Phase Shift Masks. There are many challenges to overcome before 157nm lithography can be used in high-volume manufacturing. The challenges include the development of large supplies of large diameter, high-purity CaF_2 crystals for optics; the development of pellicles with high transparency at 157nm to protect masks, and the development and commercialization of 157nm resists.

Although there are many challenges to 157nm lithography development, there has been excellent progress in the last few years. Suppliers have developed 157nm optical designs; materials for 157nm mask blanks are now available; and 157nm resists with good imaging capability have been demonstrated (Figure 6).

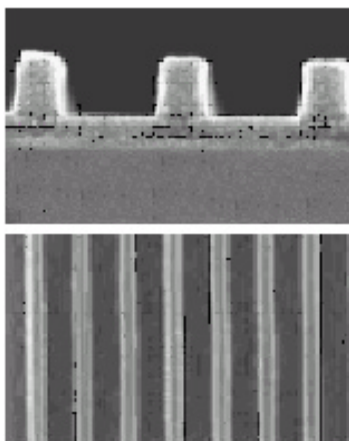


Figure 6: 157nm resist images (80nm lines)

The current forecast is that 157nm exposure tools will not be available until 2004. Therefore, 65nm integrated circuit technology will be developed using 193nm lithography. It is likely that 193nm lithography will also be used for early 65nm generation production. However, 157nm is expected to intersect the peak of the 65nm integrated circuit generation.

Extreme Ultra-Violet (EUV) lithography is being developed for 45nm generation integrated circuits. There has been excellent progress on EUV lithography in the past two years. The feasibility of manufacturing EUV optics has been demonstrated. EUV masks have been produced by several mask shops. EUV resists are available, since DUV resists are capable of EUV imaging. The EUV LLC (Limited Liability Company) has demonstrated that all the components of EUV technology can be integrated into a fully functional, 0.10NA, prototype EUV exposure tool (Figure 7), which can pattern 70nm features (Figure 8). The success of the prototype tool demonstrates that sub-50nm lithography will be possible with first-generation, production EUV exposure tools and that ~20nm lithography should be possible with second-generation EUV tools.

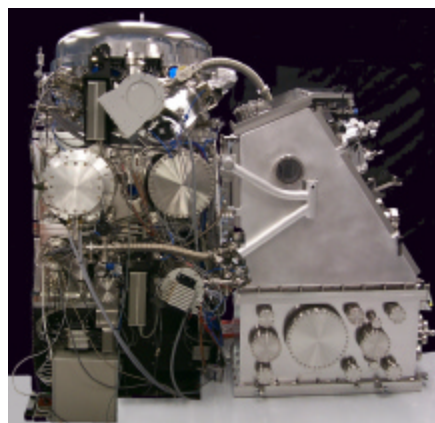


Figure 7: Prototype EUV exposure tool

However, there are still significant risks which could delay the introduction of EUV. For example, the lack of a high-power source of EUV radiation could reduce the run rate (output) of EUV exposure tools and make EUV too expensive for high-volume manufacturing. Thus, even with the excellent progress on EUV lithography, which has occurred over the past two years, the situation at the 45nm node is similar to the situation at the 65nm node.

Although there is a strong consensus that EUV lithography will be used at the 32nm generation and

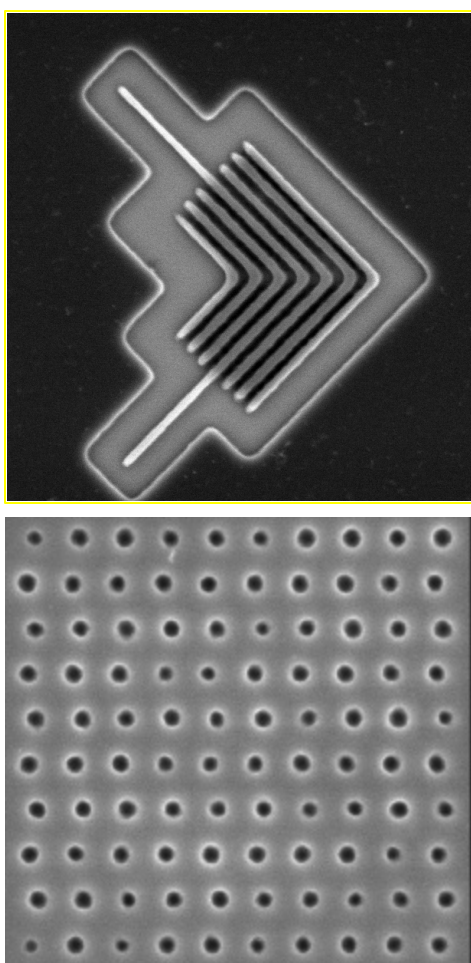


Figure 8: 70nm lines and contacts patterned with a 0.1NA prototype EUV exposure tool

below, there is significant concern as to whether EUV lithography will be ready for the 45nm generation. If EUV lithography is not ready, then 157nm lithography with Alternating Phase Shift Masks will be used for the 45nm generation.

In addition to 193nm, 157nm, and EUV lithography, Electron Projection Lithography (EPL) has been proposed for the 65nm node and below. There have also been proposals to use EPL as a complementary technology, specifically for patterning contact layers.

Although Intel continues to monitor the development of EPL technology, we do not see a place for EPL on the Intel roadmap. In particular, the low run rate of EPL tools will make the technology expensive. In addition, no one has

demonstrated that full-size EPL masks can be fabricated with the low (zero) defect levels required for production. (There are similar concerns about defects on EUV masks. However, the mask industry has a clear, data-driven roadmap to achieve zero defect EUV masks in the 2005/2006 time frame when they will be required for process development). Finally, the successful patterning of 70nm contacts (Figure 8) with 0.10NA EUV optics show that a specialized tool for patterning contacts will not be required.

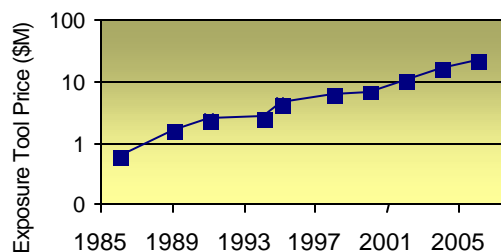


Figure 9: Exposure tool price trend

AFFORDABILITY

In 1986, Intel’s first 150mm (6”) factory was built and filled with manufacturing equipment for just over \$25M. Today (2002) the typical price for a 193nm exposure tool is approximately \$12M. The price of 157nm exposure tools is forecast to be as high as \$20M; Extreme Ultra-Violet (EUV) exposure tools may cost as much as \$25M (Figure 9). Fortunately, some of the price increases for lithography equipment have been offset by faster run rates (higher output per tool). As a result of higher tool output, the cost of Deep Ultra-Violet (DUV) lithography has actually decreased by ~20% since its introduction in the mid-1990s (Figure 10).

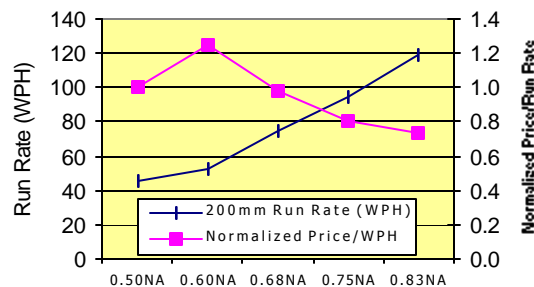


Figure 10: DUV exposure tool run rate trend

“Reuse” of lithography equipment allows the high cost of exposure tools to be spread over several generations of technology. Intel has a well-defined reuse “waterfall”

where tools that were originally purchased for patterning critical device layers are reused on subsequent process generations to pattern looser layers (Figure 11).

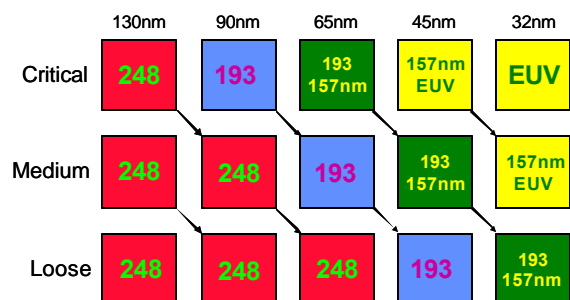


Figure 11: Intel reuse waterfall

Thus far, Intel has been able to maintain a fairly level cost for lithography by adopting the following strategy:

Rapid transition to each new generation of lithography equipment; i.e., shorter wavelengths.

Using fast (high-run rate) lithography tools.

Reusing lithography equipment over multiple process generations.

Our expectation is that this strategy will allow lithography to continue to be affordable into the 45nm technology generation and beyond.

CONCLUSION

Although the transition to sub-wavelength patterning has accelerated the rate of introduction of new lithography technologies, the necessary technology does exist and will be available when needed by the semiconductor industry. In particular, 193nm lithography will be introduced into high-volume manufacturing in 2002. There are no technological barriers to the introduction of 157nm and Extreme Ultra-Violet (EUV) lithography in the 2005 to 2007 time frame. Finally, faster and higher-output exposure tools, combined with the practice of selective reuse of existing lithography equipment, will ensure that lithography remains affordable for the foreseeable future. There is no doubt that lithography will continue to play its pivotal role in enabling Moore's Law.

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AUTHOR'S BIOGRAPHY

Peter Silverman is an Intel Fellow and Director of Lithography Capital Equipment Development. Peter joined Intel in 1978 and has held positions in process development, manufacturing, and engineering management. He is responsible for the coordination of Intel's Lithography Roadmap and for the technical and commercial management of lithography equipment development programs. Peter received a B.S. degree in Physics from MIT and a Ph.D. degree in Solid State Physics from the University of Maryland. His e-mail is Peter.J.Silverman@intel.com

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